Amendment to Claims

1 (original). A method for fabricating a nonvolatile memory, the method comprising:

(1) forming a first conductive gate for a nonvolatile memory cell;

(2) after the operation (1), forming conductive floating gates FG1 and FG2 for the memory cell.

2 (original). The method of Claim 1 wherein the operation (2) further comprises forming conductive gates CG1 and CG2 for the memory cell, wherein the gates CG1, CG2 are insulated from each other and from the first conductive gate.

3 (original). The method of Claim 2 wherein the gate CG1 overlies the gate FG1, and the gate CG2 overlies the gate FG2.

4 (original). The method of Claim 1 wherein the first conductive gate and the gates FG1 and FG2 overlie a semiconductor substrate and are insulated from the substrate;

wherein the memory cell comprises two source/drain regions in the substrate and a channel region extending between the two source/drain regions under the gates FG1 and FG2 and the first conductive gate.

5 (currently amended). The method of Claim 1 wherein a width of the ~~fist~~ first conductive gate is smaller than the minimum photolithographic line width.

6 (currently amended). The method of Claim 1 wherein a width of the ~~fist~~ first conductive gate is smaller than the width of any one of gates FG1, FG2.

7 (original). The method of Claim 1 wherein forming the first conductive gate comprises:

forming a conductive layer; and

etching the conductive layer;

wherein the etching operation comprises horizontal etching to reduce the width of the first conductive gate.

8 (original). The method of Claim 1 wherein forming the first conductive gate comprises:

forming a conductive layer;

etching the conductive layer to form a conductive feature having sidewalls;

reacting the material of the sidewalls with another material to form a reaction product on the sidewalls; and

removing the reaction product.

9 (original). The method of Claim 8 wherein the reacting operation comprises oxidation of the material of the conductive layer to form an oxide on the sidewalls.

10 (original). The method of Claim 8 further comprising, after removing the reaction product on the sidewalls, oxidizing the sidewalls to form a dielectric on the sidewalls to insulate the first conductive gate from the gates FG1 and FG2.

11 (withdrawn). The method of Claim 1 wherein the nonvolatile memory cell is part of an array of nonvolatile memory cells, each memory cell of the array having conductive floating gates FG1 and FG2 and a first conductive gate;

wherein the method comprises, before the operation (1), performing the following operation:

(a) forming one or more substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

wherein the operation (1) comprises:

(b) forming one or more conductive lines G1, each conductive line G1 overlying at least one active area, wherein each first conductive gate comprises a portion of a line G1;

wherein the operation (2) comprises:

(c) forming a layer ("FG layer") over the first conductive lines and the substrate isolation regions, wherein each of the floating gates FG1, FG2 of each memory cell comprises a portion of the FG layer;

(d) partially removing the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each conductive line G1.

12 (withdrawn). The method of Claim 11 wherein the operation (d) is terminated with reference to a time of detecting that the substrate isolation regions have been exposed.

13 (withdrawn). The method of Claim 12 wherein each substrate isolation region traverses the memory array, and each conductive line G1 crosses over plural substrate isolation regions.

14 (withdrawn). The method of Claim 11 wherein the top surface of each line G1 is planar but the bottom surface of each line G1 goes up and down over the substrate isolation regions.

15 (withdrawn). The method of Claim 11 further comprising, before forming the FG layer, forming a dielectric over sidewalls of each conductive line G1 to insulate the conductive lines G1 from the floating gates.

16 (withdrawn). The method of Claim 15 wherein each memory cell further comprises two second conductive gates insulated from the first conductive gate and the floating gates FG1 and FG2, and the method further comprises:

(e) after the operation (d), forming a dielectric D1 over the FG layer;

(f) forming a layer G2 over the dielectric D1, wherein each second conductive gate comprises a portion of the layer G2;

(g) partially removing the layer G2 and the FG layer to form the floating gates and to form from the layer G2 one or more conductive lines for the second conductive gates, wherein each second conductive gate comprises a portion of a conductive line formed from the layer G2.

17 (withdrawn). The method of Claim 16 wherein in the operation (f), the layer G2 is formed to have a portion P1 protruding above each conductive line G1; and

the operation (g) comprises:

(g1) forming a layer L1 over the layer G2 such that the protruding portions P1 of the layer G2 are exposed and not completely covered by the layer L1;

(g2) at least partially removing the protruding portions P1 of the layer G2 to form a gap in the layer G2 over each line G1, wherein at a conclusion of this removing operation a portion of the layer G2 remains covered by the layer L1;

(g3) forming a layer L2 on the layer G2 adjacent to the gaps; and

(g4) removing at least parts of the layers L1 and G2 selectively to the layer L2.

18 (withdrawn). The method of Claim 17 wherein the operation (g1) comprises:

forming the layer L1 over the entire layer G2; and

planarizing the layer L1 to expose the protruding portions P1.

19 (withdrawn). The method of Claim 17 wherein the operation (g3) comprises reacting the layer G2 with another material to form the layer L2.

20 (withdrawn). The method of Claim 19 wherein the reacting operation comprises oxidation of the layer G2.

21 (withdrawn). The method of Claim 19 wherein the reacting operation comprises a chemical reaction of the layer G2 with a metal, and the chemical reaction is followed by removal of non-reacted metal.

22 (withdrawn). The method of Claim 17 further comprising, after the operation (g4):

removing the layer L2 to expose an underlying surface of the layer G2; and

reacting the exposed surface of the layer G2 with a conductive material to form a conductive layer on the surface of the layer G2.

23 (withdrawn). The method of Claim 22 wherein the conductive layer has a lower resistivity than the layer G2.

24 (withdrawn). The method of Claim 22 further comprising, before the reacting operation, forming dielectric on at least portions of sidewalls of the layer G2, wherein the conductive layer is formed selectively on the exposed surface of the layer G2 but not on the dielectric.

25 (withdrawn). The method of Claim 22 wherein the reacting operation comprises a reaction with a metal.

26 (withdrawn). The method of Claim 22 wherein:

the first conductive gate is part of a first conductive line that provides first conductive gates to a plurality of nonvolatile memory cells;

each of the second conductive gates is part of a second conductive line that provides second conductive gates to said plurality of the memory cells;

the portion P1 and the conductive layer extend along the first conductive line through said plurality of the memory cells, the conductive layer reducing the sheet resistance of the second conductive lines.

27 (withdrawn). The method of Claim 22 wherein the memory cell comprises a source/drain region in the semiconductor substrate, and the conductive layer forms on the source/drain region.

28-50 (canceled).